LISTING OF CLAIMS

1-43. (Canceled)

44. (**Currently Amended**) An apparatus comprising:

a memory element directly coupled to a local memory bus, the local memory bus separate from the system memory bus, the memory element to be addressable via the system memory bus;

an on-board processor having an arbiter to arbitrate the system memory bus, including monitoring the system memory bus for a reserved memory address and issuing a control signal, **the on-board processor to perform processing on data from the memory element concurrently with a processor on the host system performing processing, if the local memory bus is switched to the on-board processor**; and

a switch coupled to the local memory bus, the on-board processor, and the system memory bus, to receive the control signal and selectively switch the local memory bus, in response to the control signal, to the on-board processor to switch control of the memory element to the on-board processor, and to the system memory bus to switch control of the memory element to the host system.

45. (Previously Presented) The apparatus of claim 44, wherein the switch to switch the local memory bus to the system memory bus further comprises the switch to interconnect the local memory bus to the host system via one of multiple system memory card slots.

46. (Previously Presented) The apparatus of claim 45, wherein the switch to interconnect the local memory bus to the host system via one of the multiple system memory card slots comprises the apparatus to occupy a dual inline memory module (DIMM) slot, and the switch to interconnect the local memory bus to interconnect pins of the DIMM slot.

47. (**Currently Amended**) The apparatus of claim 44, wherein ~~**the**~~ **to** selectively switch the local memory bus comprises the switch, by default, to switch the local memory bus to the system memory bus.

48. (**Canceled**)

49. (**Currently Amended**) The apparatus of ~~**claim 48**~~ **claim 44**, wherein the on-board processor to perform processing comprises the on-board processor to perform hardware acceleration of a computationally intensive task to be performed on data in the memory element.

50. (**Canceled**)

51. (**Currently Amended**) A method comprising:

initializing a circuit coupled to a host system bus, the circuit having reserved memory location and control logic, the reserved memory locations coupled to the control logic via an internal bus;

monitoring the host system bus for a signal indication an address of one or more of the reserved memory locations; and

selectively coupling the internal bus to the host system bus to switch control of the indicated reserved memory location to the host system bus**, including disabling error correcting codes prior to switching control of the reserved memory location to the host system bus**, or **coupling the internal bus** to the control logic to switch control of the indicated reserved memory location to the control logic, depending on whether the signal having the address is detected.

52. (Previously Presented) The method of claim 51, wherein selectively coupling the internal bus to the host system bus depending on whether the signal having the address is detected further comprises:

coupling the internal bus to the host system bus to switch control of the indicated reserved memory location to the host system bus if the address comprises a first address; and

coupling the internal bus to the control logic to switch control of the indicated reserved memory location to the control logic if the address comprises a second address.

53. (**Canceled**)

54. (Previously Presented) The method of claim 51, wherein monitoring the host system bus comprises monitoring control, address, and data signals on the host system bus.

55. (Previously Presented) The method of claim 51, further comprising detecting a write or a read signal indicating the address of the reserved memory location.

56. (**Currently Amended**) An article of manufacture comprising a machine accessible medium having content to provide instructions to cause a machine to perform operations including:

initializing a circuit coupled to a host system bus, the circuit having reserved memory locations and control logic, the reserved memory locations coupled to the control logic via an internal bus;

monitoring the host system bus for a signal indicating an address of one or more of the reserved memory locations; and

selectively coupling the internal bus to the host system bus to switch control of the indicated reserved memory location to the host system bus**, including disabling error correcting codes prior to switching control of the reserved memory location to the host**

system bus, or **coupling the internal bus** to the control logic to switch control of the indicated reserved memory location to the control logic, depending on whether the signal having the address is detected.

57. (Previously Presented) The article of manufacture of claim 56, wherein the content to provide instructions to cause the machine to perform selectively coupling the internal bus to the host system bus depending on whether the signal having the address is detected further comprises the content to provide instructions to case the machine to perform:

coupling the internal bus to the host system bus to switch control of the indicated reserved memory location to the host system bus if the address comprises a first address; and

coupling the internal bus to the control logic to switch control of the indicated reserved memory location to the control logic if the address comprises a second address.

58. (**Canceled**)

59. (Previously Presented) The article of manufacture of claim 56, wherein the content to provide instructions to cause the machine to perform monitoring the host system bus comprises the content to provide instruction to cause the machine to perform monitoring control, address, and data signals on the host system bus.

60. (Previously Presented) The article of manufacture of claim 56, further comprising the content to provide instructions to cause the machine to perform detecting a write or a read signal indicating the address of the reserved memory location.

61. (**New**) An apparatus comprising:

a memory element attached to a local memory bus, the memory element to be addressable via a host system memory bus, the host system memory bus separable from the local memory bus;

a processing element to arbitrate the host system memory bus and perform processing on data stored in the memory element concurrently with a host system processor processing data, the processing element to monitor the host system memory bus for a reserved memory address and issue a control signal;

a connector to interconnect to the host system memory bus via a memory card slot that resides on the host system memory bus; and

a switching element coupled to the local memory bus, the processing element, and the connector, to receive the control signal and, in response to the control signal, selectively couple the local memory bus to the processing element to switch control of the memory element to the processing element, and to the host system memory bus to switch control of the memory element to the host system processor.

62. (**New**) The apparatus of claim 61, wherein the connector comprises pins to interconnect to a dual inline memory module (DIMM) slot.

63. (**New**) The apparatus of claim 61, the switching element to couple the local memory bus to the host system memory bus by default, and to couple the local memory bus to the processing element when the reserved memory address is detected.

64. (**New**) The apparatus of claim 61, wherein to perform processing on data stored in the memory element concurrently with the host system processor processing data comprises to perform hardware acceleration of a computationally intensive task that involves data stored in the memory element.